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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,518	03/02/2000	Jacques Wong	52352-317	4862
20277	7590	12/22/2004	EXAMINER	
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, N.W. WASHINGTON, DC 20005-3096			THOMPSON, ANNETTE M	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office Communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/517,518

Applicant(s)

WONG ET AL.

Examiner

A. M. Thompson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 2,3 and 5-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2,3 and 5-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 March 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. In the Decision on Appeal rendered by the Board of Patent Appeals and Interferences in the instant case, claims 2, 3, and 5-17 were considered allowable. However, upon further review, the metes and bounds of Applicants' claims and disclosure with respect to the prior art of synthesis, and in particular, bottom-up synthesis, requires clarification for accuracy. With this objective in mind, and with the authorization of the Technology Center 2800 Director Dwyer, PROSECUTION IS HEREBY REOPENED.

2. A new ground of rejection is set forth, *infra*. Claims 2, 3, and 5-17 are pending.

### *Drawings*

3. The drawings are objected to under 37 CFR 1.83(a) because Figure 2 fails to show the production of a sub-module netlist in blocks 34A, 34B, and 34C. 34A-C only shows "GATES" which is insufficient to convey the what is stated in Applicants' specification in the last paragraph of page 3 (as amended), i.e. that sub-module netlists are produced. Figure 2 also fails to show that a top-level design netlist is created as stated in Applicants' specification at page 4, lines 3-9. Additionally, Figure 2 fails to disclose that sub-modules A, B, and C undergoes an iterative process in order to meet the timing requirements of the input and output signals as stated in the last paragraph of page 3 of Applicants' specification. Figure 3 fails to show the generation of a logic gate netlist that is the output of the synthesis process as stated in Applicants' specification at page 4, lines 21-24. Additionally, the output of the decision block #58 should return to the input arrow to block #50, to accurately depict to which process a return is being

made. Figure 4, steps 68A, 68B, and 68C must be amended to accurately reflect Applicants' invention. Examiner suggests the addition of the word "Final" after "Generate" in all three instances; an initial gate level netlist is already produced by steps 64A, 64B, and 64C. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### ***Specification***

4. The disclosure is objected to because of the following informalities: Applicants' specification at page 4, lines 21-23, states that the synthesis/optimization process

generates a logic design *and* a logic netlist. However, the process of synthesis produces a logic design netlist *or* a logic netlist.

Appropriate correction is required.

***Claim Objections***

5. Claims 5, 10 and 13 are objected to because of the following informalities: Pursuant to claims 5 and 13, at line 3, "the individual sub-blocks" lack sufficient antecedent basis. Pursuant to claim 10, at end of line 5, insert a semicolon; at line 6, pluralize "sub-module". Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the **first** paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claims 2, 3, and 5-17** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims 2 and 10 recite the limitation of "generating gate-level netlists for the gate-level designs of each of the sub-modules". Applicants' specification does not provide enablement for this limitation. Applicants' specification at page 4, lines 21-30, provides enablement for "generating the logic design and a logic gate netlist for the sub-module". However, this does not substantively correspond with Applicants' claim of "generating gate-level netlists for the gate-level designs of each of

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the sub-modules". Furthermore, a typical synthesis process does not, as Applicants' specification discloses "generate the logic design and a logic gate netlist for the sub-module." Rather, a typical synthesis process generates logic gate netlists for the logic design of sub-modules.

8. Claims 2, 3, and 5-17 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for synthesizing gate-level designs, does not reasonably provide enablement for the claim 2 and 10 limitations of generating gate-level netlists for gate-level designs. The specification does not enable a person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Applicants' specification purportedly intends to describe a "typical flow of synthesis" (page 4, line 19). Subsequently, Applicants' specification proceeds to actually disclose an atypical synthesis process in which the "synthesis/optimization process. . . generate[s] the logic design and a logic gate netlist" (page 4, lines 21-23). But, any typical synthesis flow, indeed the product of all synthesis processes in the art of integrated circuit design, produces only a gate level **netlist**. This typical synthesis flow is non-analogous to the atypical synthesis process as disclosed by Applicants. Further, Applicants' specification is silent, ergo, non-enabling, with respect to the steps involved in the atypical synthesis process.

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**Conclusion**

9. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

10. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop \_\_\_\_\_

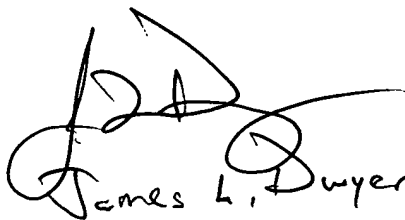
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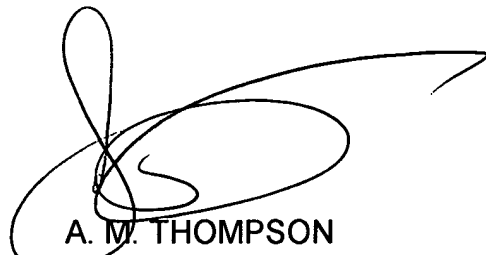
P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

  
James L. Dwyer  
Director TC 2800

  
A. M. THOMPSON  
Primary Examiner  
Technology Center 2800